

COMPUTER SYSTEM

FIELD OF THE INVENTION

This invention concerns a one-chip type computer system equipped with a memory information copy preventing function.

BACKGROUND OF THE INVENTION

Generally, in a one-chip type computer system, such as a microcomputer, for example, software is tested and debugged and the operation of the hardware is checked by an in-circuit emulator.

In this type of emulation, the program (target program) is executed by a computer system which becomes the target of the emulation, which is the target system, the pattern of optional execution information is detected by the tracing function during that execution, the target program is interrupted at an intended break point by the breaking function in order to check the state of each part within the system, and the software and hardware of the target system are checked and debugged.

In many emulators of this type, the memory contents of the major memories and registers within the target system are read out by the scan-path method.

The scan-path method will be explained with FIG. 4. In FIG. 4, the target system 100 is a microprocessor or a DSP (digital signal processor), for example, and various kinds of registers are distributed in each part and arranged within. Among these

various kinds of registers, registers that make up the major part of the system, such as registers for the address system and registers for the control system, for example, and registers for the data system, such as an accumulator register and a memory I/O register, for example, that specify the register names by commands from the program and write data to or read data from these (I/O registers), are integrated into a scan-path ①.

Each of the registers that are integrated into the scan-path is structured to input and output data in parallel in normal mode and input and output data serially in the scan-path mode.

Generally, one scan-path is provided within one computer system, and a number of registers are serially connected in this scan-path. For example, in the target system 100 in FIG. 4, 7 registers RA1, RA2, RB1, RB2, RB3*, RC1, and RC2 are serially connected in the scan-path (1). These registers RA1, RA2, RB1, RB2, RB3, RC1, and RC2 are accessed in parallel in normal operations, and all of these are serially accessed when the scan-path is used. Both ends of this scan-path ① are connected to the emulator 110 through multiplexers 102 and 104 and data input and output terminals 106 and 108.

Also in FIG. 4, the register bypass is a register that is used when bypass is performed without using the scan-path in the emulation mode. A number of ICs are mounted on the same printed substrate, and when one IC is debugged by the scan-path, other IC's bypass signals via the aforementioned register bypass. Both ends of this bypass 2 are connected to the emulator 110 through

* Translator's note: RB3 is mislabeled in FIG. 4.

In this way, the danger of the ROM information of the system being illegally copied remains because of the scan-path function.

When the secrecy of the ROM information had to be maintained in a computer system of this type, the signal path for connecting the interface circuit within the system relative to the emulation and the external emulation was interrupted by the hardware, and signals could not be exchanged between them.

However, in this method, the signal path was completely interrupted once copy protection was applied, and there was the inconvenience that debugging and testing afterwards could not be performed at all.

The aim of this invention, which was made while considering said problem, is to offer a computer system in which execution or cancellation of copy protection can be switched at any time in a simplified structure.

Also, another aim of this invention is to offer a computer system that has a copy protection function with a high level of security and flexibility.

SUMMARY OF THE INVENTION

In attaining the aforementioned aims, the first^{aspect of a} computer system of this invention, which is a computer system in which a processor, memory, peripheral circuits, and interconnecting wires are formed together over one semiconductor substrate, has a structure equipped with: a scan-path interface circuit, which allows for a readout of the storage contents of a prescribed memory or a register within the system through the

aforementioned processor by the scan-path method; a switching circuit, which can be accessed by the aforementioned processor, and selectively switches the aforementioned scan-path interface circuit between the enabled state and the disabled state according to the prescribed switch control information given by the aforementioned processor; and a program storage means, which stores the program for the aforementioned processor to enable processing to give the aforementioned switch control information to the aforementioned switching circuit.

Also, ^a ~~the~~ ^{aspect of a} second computer system of this invention in the aforementioned first computer system has a structure in which the aforementioned switching circuit has: a register for holding the aforementioned switch control information which can be accessed by the aforementioned processor; and a gate circuit, which is provided over a signal path that is connected to the aforementioned scan-path interface circuit and has an open state or a closed state according to the contents of the aforementioned register.

^A ~~The~~ ^{aspect of a} third computer system in this invention in the aforementioned first computer system has a structure in which the aforementioned switching circuit has: a number of password registers for holding the aforementioned switch control information which can be individually accessed by the aforementioned processor; a comparison means, which compares the contents of the number of aforementioned password registers with each other and yields comparison results; and a gate circuit, which is provided over the signal path which is connected to the aforementioned scan-path interface circuit, and which has an

open state or a closed state according to the comparison results from the aforementioned comparison means.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing the chief components of the computer system in an embodiment of this invention.

FIG. 2 is a circuit diagram showing a constitutional example of the switching circuit in the embodiment.

FIG. 3 is a circuit diagram showing a modified example of the switching circuit in the embodiment.

FIG. 4 is a diagram which explains the scan-path method.

In the figures, 10 represents DSP, 12 ROM, 14 RAM, 16 gate array unit, 18 scan-path interface circuit, 20 host interface circuit, 24 switching circuit, 30, 32 password registers, 34 comparator, 36 gate circuit, and 38 register.

DESCRIPTION OF EMBODIMENTS

An embodiment of this invention will be explained by referring to FIGS. 1-3 below.

FIG. 1 shows the chief components of a computer system in an embodiment of this invention. This computer system is a one-chip type microcomputer, in which a processor, memory, peripheral circuits, and interconnecting wires are formed together over one semiconductor substrate.

In this system, the processor consists of a universally used DSP 10, the memory consists of a mask ROM 12 and an internal RAM (random-access memory) 14, and peripheral circuits consist of a gate array unit 16 and a host interface circuit 18, for example. The gate array unit 16 includes: a host interface circuit 20; a universally used interface circuit 22; a switching circuit 24; and other various kinds of custom logic circuits (not shown in the drawing).

The ROM 12 stores programs that specify the processing operations of the DSP 10, various kinds of settings data and/or tables, for example. The program in relation to the copy protection (routine) by this embodiment, which will be described later, may be stored in the ROM 12. The DSP 10 and the ROM 12 are connected to each other through the program address bus PRAB and the program data bus PRDB.

The RAM 14 stores data in relation to arithmetic processing in the DSP 10, and also may store appropriate system programs or application programs in some cases. The DSP 10 and the RAM 12 are connected to each other through the program address bus PRAB, program data bus PRDB, data readout address bus DRAB, data readout data bus DRDB, data write address bus DWAB, and the data write data bus DWDB.

The host interface circuit 20 in the gate array unit 16 is an interface circuit for exchanging data and programs between this system and the host computer (not shown in the FIG.). The universally used interface circuit 22 is an interface circuit for exchanging data and programs between this system and outside circuits or the memory.

The switching circuit 24, which is provided within the gate array unit 16, is one component that makes up the copy protection function in this embodiment. The exact structure as well as the operation of this switching circuit 24 will be described later.

Each part within the gate array unit 16 is connected to the logic interface circuit 26 through external buses that include the logic address bus LAB, logic data bus LDB, and the logic control bus LCB. Then, the logic interface circuit 26 is connected to the DSP 10 through the aforementioned internal buses PRAB, PRDB, DRAB, DRDB, DWAB, and DWDB.

The logic interface circuit 26 is an interface circuit which connects each part within the gate array unit 16 to the DSP 10.

The scan-path interface circuit 18 is an interface circuit which implements the scan-path method of emulation in this system, and includes data transfer means, such as exclusive registers for the emulation and multiplexers, for example, and a controller, which controls these data transfer means according to the timing signal and control signal from the external emulator, for example.

FIG. 2 shows an example of the circuit structure of a major part of the switching circuit 24 in this embodiment.

This structural example consists of a pair of password registers 30 and 32 consisting, for example, of 16 bit parallel-in parallel-out type registers, comparator 34, and a gate circuit 36. The data input terminal of each of the password registers 30 and 32 is connected to the logic data bus LDB, and the data output terminal of each is connected to the input

terminal of the comparator 34. The output terminal of the comparator 34 is connected to the control terminal of the gate circuit 36. The gate circuit 36 consists of a logic circuit, such as an AND gate, for example, and it is provided in the signal path between the scan-path interface circuit 18 and the terminal pin for the emulation (not shown in the figure).

Also, an address decoder circuit (not shown in the figure) as a write control means for writing data into the registers 30 and 32 is provided within the switching circuit 24. This address decoder circuit is connected to the logic address bus LAB and the logic control bus LCB.

Next, the function of the copy protection function in this embodiment will be explained.

When a reset signal enters the reset terminal of this system (chip), for example, the DSP 10 executes the necessary initialization processing according to the prescribed program stored in the ROM 12, and implements the copy protection routine below as one process.

First, the DSP 10 outputs the prescribed readout address via the data readout address bus DRAB, reads out the data of the prescribed password PW via the data readout data bus DRDB from the RAM 14, and takes in this password data PW, which was read out.

Successively, the DSP 10 respectively sends out the prescribed write address, which specifies the primary register 30 within the switching circuit 24, and said password data PW over the logic address bus LAB and the logic data bus LDB through the logic interface circuit 26. In this way, said

DRAB and the data readout data bus DRDB. This password PW' may be read out from the prescribed storage address in the RAM 14, or it may be the one given together with the canceling command from the host interface circuit 20. Either way, this password PW' also is a secret code known only by those involved with this system, and it is selected to be the same value as the password PW, which is held at the primary password register (30).

Next, the DSP (10) writes the password PW', which was taken in, to the secondary password register (32) at the switching circuit (24) during the same writing cycle as the aforementioned initialization.

Then, the comparison result signal CL of the logic value H, for example, indicating that the contents of both the password registers 30 and 32 (PW, PW') match, is obtained from the comparator 34 at the switching circuit 24, and the gate circuit 36 will have an on or conductive state according to this comparison result signal CL. In this way, the signal path between the scan-path interface circuit 18 and the terminal pin for emulation is made conductive, and an enabled (operation is possible) state is obtained.

Accordingly, as the emulator is connected to this system, signals can be exchanged between that emulator and the scan-path interface circuit 18, and the scan-path method of emulation can be implemented. Through this emulation, storage information from major memories and registers within this system can be read out and debugging, and testing can be performed, and it is also possible to dump the contents from the mask ROM 12.

As described above, in the computer system in this embodiment, the switching circuit 24, which selectively switches

the scan-path interface circuit 18 between the enabled state and disabled state, is provided in the gate array unit 16, and the routine for the DSP 10 to access this switching circuit 24 and to write the switch control information (PW, RW, and PW') is pre-stored in the ROM 12.

During the normal state, the scan-path interface circuit 18 is in the disabled state when the prescribed switch control information (PW, RW) is written to the switching circuit 24 because of the copy protection routine at initialization, for example, execution of the emulation by the scan-path method is impossible, and there exists a state in which the information storage within the system, particularly the stored information of the ROM 12, cannot be copied. Also, different values can be forcibly set (through the hardware) respectively at the password registers 30 and 32 by resetting the system, and the scan-path interface circuit 18 can be in the disabled state.

Then, when it is necessary to execute the emulation in this system, for debugging, for example, a prescribed command is given by an external host controller, the copy protection canceling routine is executed within the system, the prescribed switch control information (PW, PW') is written to the switching circuit 24 and the scan-path interface circuit 18 then enters the enabled state, execution of the emulation by the scan-path method becomes possible, and the storage information within the system, particularly the storage contents of the ROM 12, can be read out.

After completion of the emulation, the DSP (10) executes the same aforementioned copy protection routine while responding

aforementioned copy protection function with a high level of security and flexibility is attained with minimal necessary resources without requiring special terminals and external circuits.

An ideal embodiment of this invention was explained above, but many modifications and alterations are possible within the range of the technological concept of this invention.

For example, various methods are possible for giving the instruction to switch between execution/cancellation of copy protection to this system from the outside. The command or password can be given from a universally used interface circuit 22 and other ports instead of via the host interface circuit 20.

It is also possible to provide more than 3 password registers at the switching circuit 24. Also, although the level of security and flexibility becomes significantly lower than that of the aforementioned embodiment, it is possible to have a structure with one register 38 and a gate circuit 36, one switch control information is written to the register 38, and switching between execution/cancellation of copy protection is controlled, as shown in FIG. 3.

The gate circuit 36 in the off state may practically shut off the signal path that is connected to the scan-path interface circuit 18, and it is not necessary to shut off all bits of said signal path. It is possible to have a structure which interrupts only the clock signal for the scan pass.

Also, in the aforementioned embodiment, the switching circuit 24 was provided in the signal path, which was connected to the scan-path interface circuit 18, but it is also possible to have a structure in which the switching circuit 24 directly

or indirectly switches the scan-path interface circuit 18 without the inclusion of such a signal path.

In the aforementioned embodiment, the routine (program) relative to copy protection is stored in the ROM 12, but it may be stored in the RAM 14 or other storage means.

In the aforementioned embodiment, the switching circuit 24 was electrically provided between the scan-path interface circuit 18 and the terminal pin for emulation, but it is also possible to provide it at other locations, such as between the scan-path interface circuit 18 and the DSP 10.

Concerning the processor in the computer system in this invention, processing by optional methods besides the DSP are possible, and various kinds of modifications are possible to the memory and peripheral devices.

As explained above, in the computer system in this invention, the scan-path interface circuit is selectively switched between the enabled state and the disabled state by execution of the prescribed program by the processor and writing in the prescribed switch control information into the switching circuit. Therefore, execution or cancellation of copy protection can be switched any time in the simplified structure, and maintenance of secrecy of information stored within the system and repetition of debugging can be attained at the same time.